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10/805,755	03/22/2004	Shinji Kuno	6639P011	1246

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Blakely, Sokoloff, Taylor & Zafman LLP
7th Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
UNELUS, ERNEST	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,755	KUNO, SHINJI	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8 and 18-30* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 18-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/16/07 has been entered.

The instant application having application No. 10/805,755 has a total of 30 claims. After the first action on the merits, claims 4-7 and 9-17 are cancelled and claim 8 are withdrawn from consideration and claims 1-3 and 18-30, which 18-30 are new, are now pending in the application; within claims 1-3 and 18-30, which are a total of 15, there are 2 independent claims and 13 dependent claims, all of which are ready for examination by the examiner.

Applicant's arguments filed 05/16/2007, with respect to the rejection(s) of claim(s) 1-3 and 18-30 under Kabenjian (US pat. 5,613,162) have been fully considered and is not persuasive.

The applicant argues that Shimizu, the cited reference, does not teach that the commands constitute of the first stream data as now claimed.

In regards to "a first processor **(Main Processor 110)** coupled to the communication bus **(the communication bus between the main processor 110 and the graphics and audio**

processor 114 of fig. 2, as discloses in col. 7, lines 25-31. see fig. 2), the first processor to decode a first stream data including video data and audio data routed over the communication bus" **(see col. 6, line 64 to col. 7, line 3, which discloses the main processor generating a command and using the graphics and audio processor to transmit this to an audio codec 122. See col. 6, line 64 to col. 7, line 3, which discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". See also fig. 4 and col. 4, lines 18-41, which discloses the Graphics Audio Processor 114 receiving video and audio command from the Main Processor 110)**;

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4a. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4b. **Claims 1-3, 18-19, 21, 23-25, and 28-30,** are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al. (US pat. 6,609,977).

5. As per **claim 1**, Shimizu discloses "An apparatus **(system 50 of fig. 2)** comprising:

a drive device **(mass storage access device 106 of fig. 2, as discloses in col. 6, line 59)**; a communication bus **(the communication bus between the main processor 110 and the graphics and audio processor 114 of fig. 2, as discloses in col. 7, lines 25-31)**;

a first processor **(Main Processor 110)** coupled to the communication bus **(see fig. 2)**, the first processor to decode a first stream data including video data and audio data routed over the communication bus **(see col. 6, line 64 to col. 7, line 3, which discloses the main processor generating a command and using the graphics and audio processor to transmit this to an audio codec 122. see col. 6, line 64 to col. 7, line 3, which discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". See also fig. 4 and col. 4, lines 18-41, which discloses the Graphics Audio Processor 114 receiving video and audio command from the Main Processor 110)**;

a second processor **(Graphics and Audio Processor 114)** provided with a second stream data including video data and audio data **('audio output of mass storage access device 106')** received from the drive device without being routed over the communication bus **(col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**, the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus **(in regards to this limitation, fig. 2, shows the audio codec to decode the 'audio output of mass storage access device 106'. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor generates instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor processes I/O. Also, as disclose in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command**

processor is inside the graphics and audio processor. See also col. 6, lines 56-59 for further detail).

6. As per **claim 2**, Shimizu discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]** "wherein the second processor is a stream processor" **(col. 7, lines 13-17 discloses the graphics and audio processor to be processing audio stream, as also discloses in fig. 2).**

7. As per **claim 3**, Shimizu discloses wherein the first processor is a central processing unit (CPU) **(see col. 6, line 50)**.

8. As per **claim 18**, Shimizu discloses wherein the drive device is a hard disk drive **(see hard disk drive 62 of fig. 2).**

9. As per **claim 19**, Shimizu discloses wherein a network control unit **(controllers 52, as discloses in fig. 1)** coupled **(col. 6, lines 25 –27, discloses that it can be coupled wirelessly or through a cables)** to the communication bus **(see fig. 1)**, the network control unit to transmit the first stream data via the communication bus **(see col. 6, lines 53-55, which discloses "In this example, main processor 110 (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers 52", which causes the main processor to transmit a command, using the communication bus, to audio processor 114)**.

10. As per **claim 21**, Shimizu discloses wherein the second stream data **('audio output of mass storage access device 106')** includes video data and audio data **(col. 6, line 29 discloses the storage medium 62 of fig. 2 being a video game; also, col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106)")**.

11. As per **claim 23**, Shimizu further discloses: a video bus **(the communication bus between the main processor video/encoder 120 and the graphics and audio processor 114, as discloses in fig. 2)**; and a graphic controller **(Graphics and Audio Processor 114), which has a 3D Graphics processor)** in communication with the first processor and the second processor **(see fig. 3)**, the graphic controller to convert the decoded first stream data into display video signals and to transmit the display video signals to the second processor over the video bus **(see fig. 3)**.

12. As per **claims 24 and 29**, Shimizu discloses wherein the second processor superposes the display video signals transmitted over the video bus on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor over the communication bus **(see fig. 2 and col. 7, lines 13-17, which discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio**

signals the processor generates and/or receives via a streaming audio output of mass storage access device 106)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor, it generate instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor to process I/O. as also discloses in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command processor is inside the graphics and audio processor).).

13. As per **claims 25 and 30**, Shimizu discloses wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen **(see col. 57 line 36 to col. 58, line 8)**.

14. As per **claim 28**, Shimizu discloses "An apparatus **(system 50 of fig. 2)** comprising:

a communication bus **(the communication bus between the main processor 110 and the graphics and audio processor 114, as discloses in col. 7, lines 25-31)**;

a drive device **(mass storage access device 106 of fig. 2, as discloses in col. 6, line 59)**; a video terminal **(video encoder 120 of fig. 2)**;

a first processor **(Main Processor 110)** coupled to the communication bus **(see fig. 2)**, the first processor to decode a first stream data including video data and audio data sent over the

communication bus **(see col. 6, line 64 to col. 7, line 3, which discloses the main processor generating a command and using the graphics and audio processor to transmit this to an audio codec 122. see col. 6, line 64 to col. 7, line 3, which discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". See also fig. 4 and col. 4, lines 18-41, which discloses the Graphics Audio Processor 114 receiving video and audio command from the Main Processor 110)**; and

a second processor **(Graphics and Audio Processor 114)** coupled to the drive device, the video terminal, and the first processor **(see fig. 2)**, the second processor being provided with a second stream data including video data and audio data **('audio output of mass storage access device 106')** that is sent from the drive device without use the communication bus **(col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**, the second processor to (i) decode the second stream data for reproducing the second stream data in accordance with an instruction sent from the first processor via the communication bus and (ii) display video signals, that are based

on the decoded first stream data and transmitted by the first processor over a video bus separate from the communication bus, on the video terminal **(in regards to this limitation, fig. 2, shows the audio codec to decode the 'audio output of mass storage access device 106'. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor generates instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor processes I/O. Also, as disclose in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command processor is inside the graphics and audio processor. See also col. 6, lines 56-59 for further detail).**

Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claims 20 and 22,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US pat. 6,609,977) in view of Witt (US pub. 2004/0109005).

17. As per **claim 20,** Shimizu discloses, "The apparatus according to claim 1," **[see rejection to claim 1 above]**, including a control unit but fails to specifically disclose, "wherein the control unit includes an IEEE 1394 processor".

Witt discloses wherein the control unit includes an IEEE 1394 processor **(see paragraph 0035, which discloses the IOP 700, as a control unit being an IEEE 1394 processor).**

Shimizu et al. (US pat. 6,609,977) and Witt (US pub. 2004/0109005) are analogous art because they are from the same field of endeavor of video data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game controllers as taught by Shimizu and a video processing method for preparing an anti-aliased foreground image for display over an image background as taught by Witt.

The motivation for doing so would have been because Witt teaches, "The IOP 700 has a Direct Memory Access (DMA) architecture to facilitate rapid data transfer rates" **(see paragraph 0035)**.

Therefore, it would have been obvious to combine Witt (US pub. 2004/0109005) and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 20.

18. As per **claim 22**, the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Witt further discloses, "wherein the communication bus is a Peripheral Component Internet (PC1) bus" **(see paragraph 0065).**

19. **Claims 26 and 27,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US pat. 6,609,977) in view of Ochiai et al. (US pat. 6,757,482).

20. As per **claim 26,** Shimizu discloses, "The apparatus according to claim 1," **[see rejection to claim 1 above]**, including a third stream data to the second processor for storage into a storage medium associated with the drive device **(see fig. 2 and col. 7, lines 25-31)**, but fails to specifically disclose a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device.

Ochiai discloses wherein a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device **(see col. 5, lines 23-30 and fig. 2).**

Shimizu et al. (US pat. 6,609,977) and Witt Ochiai et al. (US pat. 6,757,482) are analogous art because they are from the same field of endeavor of video data processing.
At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game controllers as taught by Shimizu and a method and a device for dynamically editing broadcast data (terrestrial or satellite) or cablecast data received by a receiving terminal (TV tuner etc.) as taught by Ochiai.
The motivation for doing so would have been because Ochiai teaches a TV tuner allow you to receive broadcast data (video data and audio data) of broadcast programs **(col. 5, lines 23-30).**

Therefore, it would have been obvious to combine Ochiai et al. (US pat. 6,757,482) and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 26.

21. As per **claim 27**, the combination of Shimizu and Ochiai discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Ochiai discloses a television tuner **(see fig. 2)** and Shimizu further discloses "a transport stream bus **(parallel bus 130 of fig. 2)** coupled to the second processor, the transport stream bus enables transmission of the third stream data to the second processor without using the communication bus" **(see col. 7, lines 25-31).**

RELEVANT ART CITED BY THE EXAMINER

22. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

23. The following reference teaches an apparatus comprising; a communication bus; a drive device; a video terminal; a first and a second processor.

U.S. PATENT NUMBER

US 6,654,827

US 6,434,645

US 6,356,968

US 5,805,933

US 5,799,036

US 7,149,208

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

24. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

25. Per the instant office action, claims 1-3 and 18-30 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

27. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

July 10, 2007

Ernest Unelus
Patent Examiner
Art Unit 2181

7/19/2007